DIGITAL CHIP FABRICATION
SNN Hardware Neuron

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INTRODUCTION

- Current lack of opportunity for chip creation, bring-up, and fabrication
- Growing environment for open-source silicon
- Lack of knowledge base

OVERVIEW

- Silicon prove a digital spiking neural network (SNN)
- Develop tutorial documentation
- Research and create bring-up plan

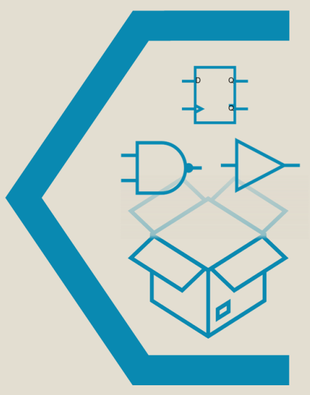
METHODOLOGY

- OpenMPW Program provides infrastructure and fabrication
- MNIST data set offers a network and test values
- Design Requirements
  - Digital configuration
  - 10 square millimeter area
  - Pass prechecks
- Documentation Requirements
  - Meticulously detailed guide for beginner level user

Manufacturing
EFABLESS

➞ Doped Silicon creates Transistors
➞ Transistors create Invertors
➞ Invertors create Logic

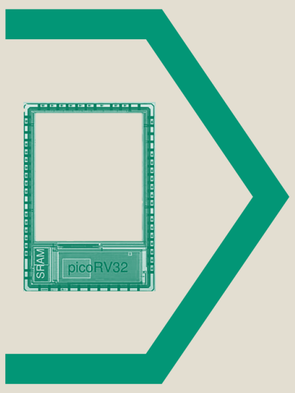
Process Design Kit
SKYWATER



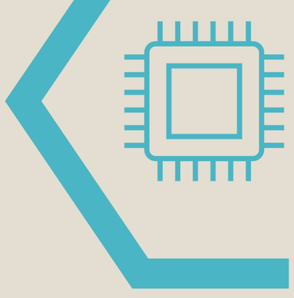
➞ Logic Combinations create Standard Cells
➞ Standard Cells are Spec-ed for Fabrication
➞ Specs Distributed as Process Design Kit (PDK)

Hardware Description
CARAVEL HARNESS / USER AREA

➞ Verilog Defines User Functionality
➞ Wrapper to Standardize Designs



ASIC Flow
OPENLANE



➞ Map Verilog to Netlist
➞ Place Cells in Area
➞ Connect Power & Clock
➞ Define Fabrication Masks

IMPLEMENTTION

Architecture:
- Input: Handwritten Digit. 9 x 9 array of brightness values. “Pixel image”
- Output: Spikes for each digit (0-9), the highest spike is the classification
- 8 states, 1 neuron unit to implement a Leaky Integrate and Fire (LIF) model

Load
- Image pixel values from MNIST
- Weights from pretrained snnTorch network
- Addresses from CPU

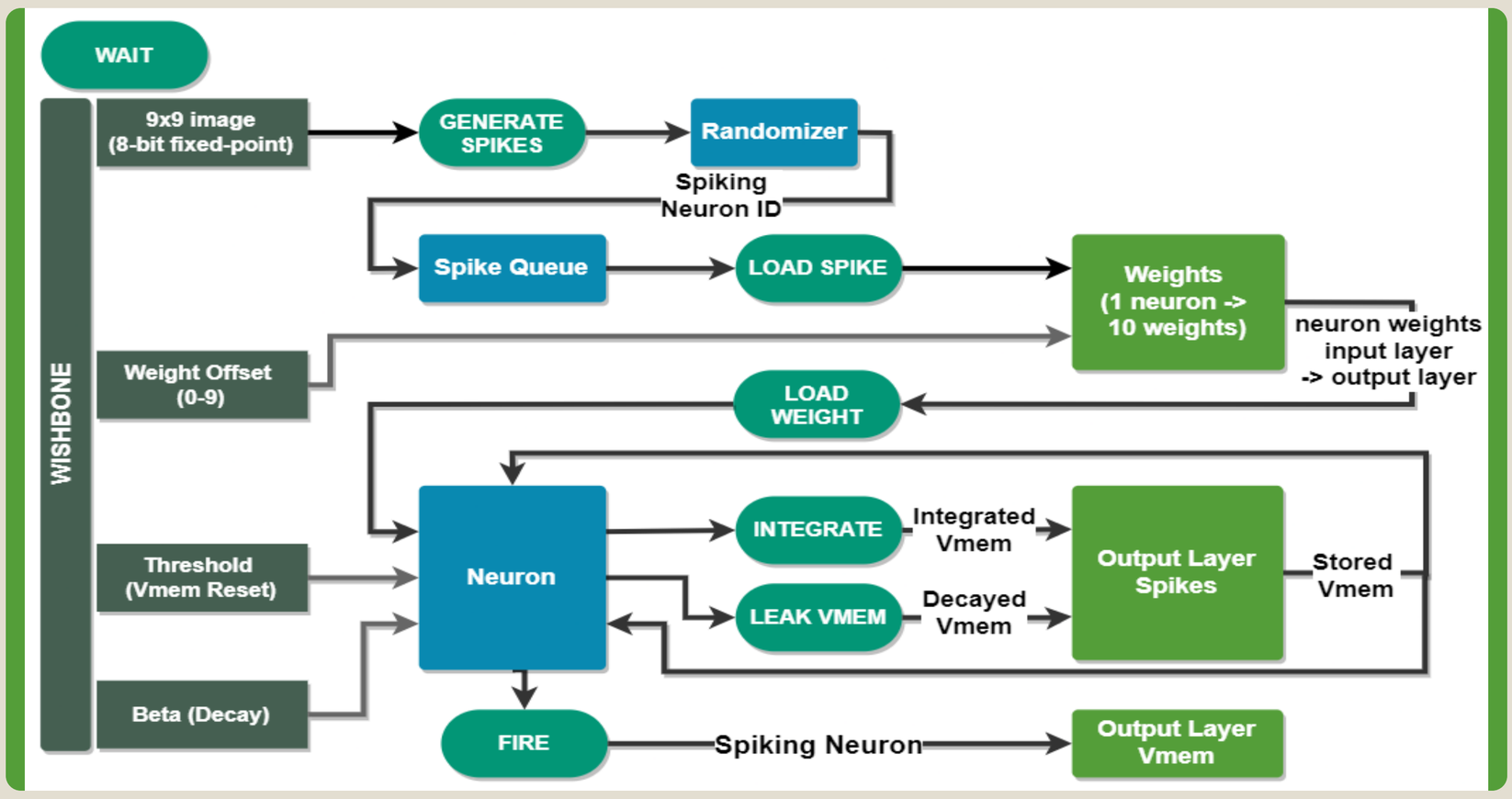
Generate
- Rate encoded quantifies number of spikes in a time interval
- Pseudo random number generator seeded with image values
- If spike – pixel “propagates”

Integrate
- Send data to neuron to add according to weights
- Build up Membrane voltage

Leak
- Leak membrane voltage each time step
- Decay is dictated by a parameter Beta

Fire
- Fire according to accumulated membrane voltage at neuron ID

Data Flow Diagram



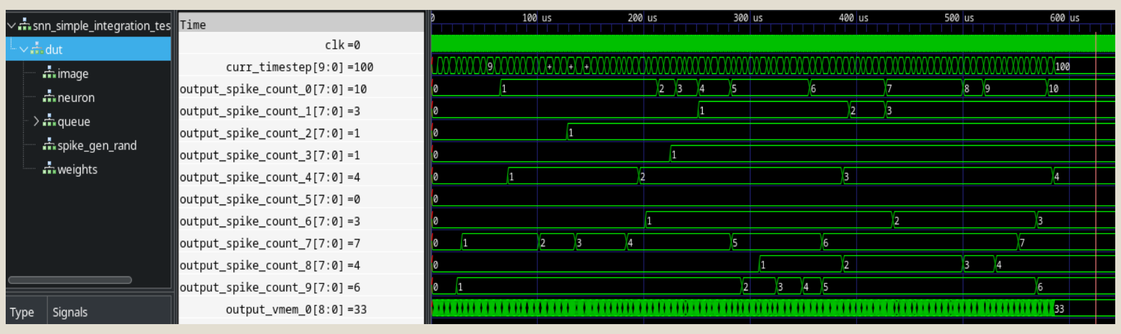
CHALLENGES/SOLUTIONS AND OUTCOMES

Understanding the Efabless Process
- Unthoroughly documented/ trouble shot
- Unavailable Shuttles

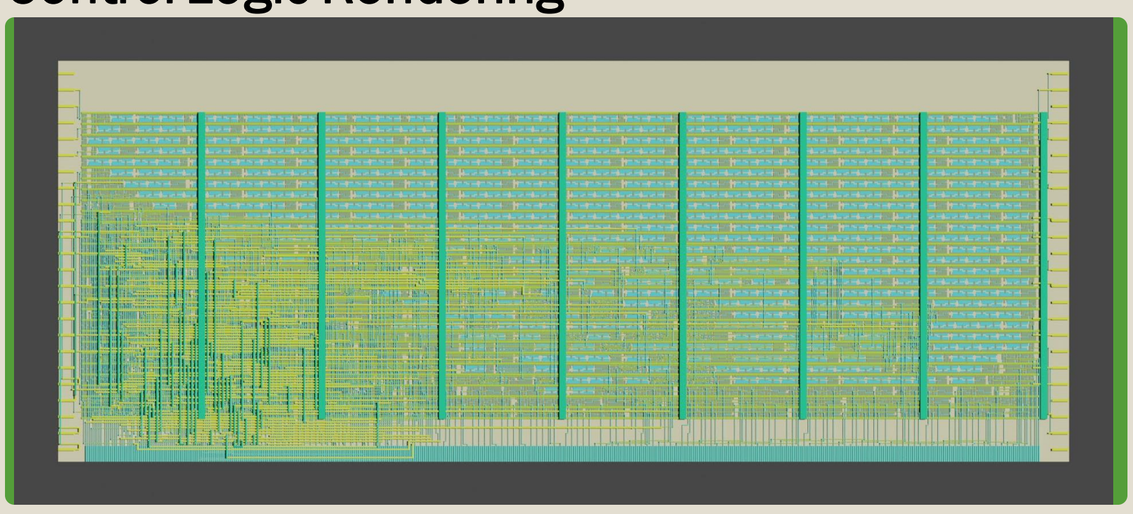
Memory Challenges
- SRAM macro
- Design usage experimentation

Space Challenges
- Downsize network in software before

Simulation Results



Control Logic Rendering



CONCLUSION

In designing a digital neuron ASIC, there were a couple major outcomes.
- Submission ready (simulated and hardened) digital neuron design
- Bring-Up plan for use when physical chip is delivered
- Public GitLab repository with SNN for community use
- 38+ Pages of Documentation Detailing:

Environment Set-Up	Getting Started	Submission
Daughter & Carrier Board	Wishbone Bus	Bring-Up
Interrupts	Logic Analyzer	GPIO

There is great potential for open-source ASICs in education and industry. This project provides a basis for future projects whether students at ISU or individuals in the Open-source SI ecosystem.

POTENTIAL APPLICTIONS

- Basis for SNN accelerator unit
- Contribution to the Open-Source Silicon Community
- Inspire and empower students in the field of digital design
- Documentation for more teams and future classes