EE/CprE/SE 492 WEEKLY REPORT 1

1/17/2023 – 2/18/2023

Sdmay23-28

Digital Chip Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Katherine Gisi: Spokeswoman, SNN neuron design, Leader

William Zogg: SNN neuron Design

Tyler Green: Software tool research, Environment setup

Aaron Sledge: Software tool research & Documentation

Fulai Zhu: Documentation

Weekly Summary

- Met with team sddec23-06 to explain the caravel harness, and general development guidelines/tips
- Updated advisor on weekly progress since he was out-of-office
- Met with team on 2/16 to discuss next steps and work on SNN design
- Met twice in the past week to inform other group members on individual progress and concerns

Past week accomplishments

1. Created a tutorial document with 5 of 14 sections filled out. The purpose of the document being for future senior design groups so that they can streamline the process of digital ASIC design through Caravel's open-source chip design community. And spend as little time learning how to use the necessary tools as possible.
2. Tested more SNN designs, decided on a design with two layers, using a queue to store spiking neurons, and memory for Vmem, spike count, and weights.

Pending Issues

1. The tutorial document is still far from complete. There are still multiple sections that need to be explained and expanded upon. Such as a logic analyzer tutorial, a wishbone bus tutorial, a Klayout tutorial etc.
2. Need to figure out how to get a layout that shows a better view of the things we placed in the caravel harness, will reach out to the slack group for help in that area. Then, we will have a better idea of how much space we have for SRAM.

Individual Contributions

NAME	Individual Contributions	Hours this week	Hours cumulative
Aaron Sledge	Created an informational document on the caravel harness. Also created a tutorial document on how to set up the environment to work with the caravel Repo. As well as instructions on how to use some of the caravel software tools.	6	27
Katherine Gisi	Created deign diagrams, revised upon description of chip, started preliminary outline of connections on an embedded system level.	6	25
Fulai Zhu	Working on characterizing the PCB (Printed Circuit Board) for design, try to find the functions of each part on caravel harness.	5	22
Tyler Green	Testing SRAM in caravel, designing tests for SRAM usage and analyzing gds layout to determine available space. Testing SNN layer designs for classification accuracy. C++ simulation of SNN design and image/weight loading. Python tool to extract images and weights from snntorch	6	30
William Zogg	Worked on SNN design including diagrams, datapaths, and control logic considerations. Researched necessary interfaces and factors needed for our design including Wishbone, SRAM, etc. Final draft of design mostly completed, save for a few considerations depending on our memory and space limitations.	6	26

Comments and Extended Discussions

(Optional)

Plans for the upcoming week

The plan for the upcoming week includes starting on the RTL Verilog, creating a list of register names and sizes for use of the wishbone bus, doing an experiment with the wishbone bus and data transfer, Klayout experimentation, Klayout tutorial videos, and continuing documentation.

Summary of weekly advisor meeting:

Due to our advisor being off campus at a conference, we were not able to hold a meeting at our regular time, but we met for an hour as a team and shared with each other current progress for the project and what our next steps were for the week. We also provided a couple paragraphs of written summary for our advisor.