EE/CprE/SE 492 Biweekly Report 4

3/25/2023 - 4/7/2023

sdmay23-28

Digital Chip Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Katherine Gisi: Spokeswoman, SNN neuron design, Leader

William Zogg: SNN neuron Design

Tyler Green: Software tool research, Environment setup, Component RTL design

Aaron Sledge: Software tool research & Documentation

Fulai Zhu: Documentation

Weekly Summary

This week saw us finishing up on the individual parts of the rtl. We had team members working still in their roles as defined above as well as some branching out as tasks wrap up.

Past week accomplishments

1. Started to write unit tests for the queue and neuron
2. Finished overall control logic for SNN

Pending Issues

We are currently not sure if an MPW-9 will be run/funded by Efabless, but the deliverables for our project to our client will remain the same, so we do not see any major issues with this. We can still develop documentation and have a project working in Caravel even if it ends up not being submitted to the program officially.

Individual Contributions

NAME	Individual Contributions	Hours this week	Hours cumulative
Aaron Sledge	Worked on understanding Tyler's test bench to assist the team in creating & speeding up the process of testing edge cases for our modules. As well as researched updates made to caravels commands and tools to see what needs to be edited in the tutorial document.	4	40
Katherine Gisi	Worked off of Tyler's simple testbench. Did research on submission options.	6	37
Fulai Zhu	Do research about how to test the Efabless board and design the bring up plan for project test.	6	39
Tyler Green	Starting a testbench template for the queue module unit test, helping Kat and Aaron begin testing of RTL	6	52
William Zogg	Continued development for our SNN control logic. Edited design several times due to updated information on randomization algorithms. Upon storage integration we can proceed to test the unit.	8	40

Comments and Extended Discussions

(Optional)

Plans for the upcoming week

1. **Keep finish the bring up plan and design the codes to test the project.**
2. **Establishing testing protocols with all cases that need to be functional including edge cases**
3. **Start looking at spots to place logic analyzer ports (as well as whatever it is that can set signals itself).**

Summary of weekly advisor meeting:

We discussed the deliverables expected by Dr. Duwe (just in case MPW-9 does not happen, but what he would like to see regardless) including:

- documentation of caravel and efabless process
- a working project in Caravel passing prechecks
- bring-up plan for board