sdmay23-28: Digital Chip Fabrication

Week 2 Report
October 1 - October 9

Team Members

Katherine Gisi — *Team Spokesperson*
Tyler Green — *Software tools for testing*
William Zogg — *Documentation / Research*
Fulai Zhu — *Documentation*
Aaron Sledge — *Documentation & Software tool reaserch*

Summary of Progress this Report

Researched caravel as well as all of the surrounding interfaces.

Researched open-source tools that might be used for this project.

Finished team contract.

Met with previous years senior design team to walk through how to harden and test simple adder in caravel harness.

Pending Issues

Need to research more about SNN.

Need to research more about opensource tools.

Still need to finalize project plan and timeline.

We all still need to set up the environment as well as learn how to harden a design in said environment.

Plans for Upcoming Reporting Period

Finalize Project timeline

Have everyone set up the environment

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Katherine Gisi	Communicated with previous team to set up meeting. Continued work on project plan wiith research on efabless process.	4	0
Tyler Green	Started new design, testing the wishbone and	4	0

	logic analyzer in an XOR module. And reorganized Gitlab repo.		
William Zogg	Worked on document and researched memory components of harness.	4	
Fulai Zhu	Help to finish the design document: Requirement.	3	
Aaron Sledge	Started and uploaded lightning talk slides for project plan, as well as reaserched a little bit about icarus verilog	5.5	

Gitlab Activity Summary

Reorganized Gitlab repo to make it easier for everyone in the group to harden and test the adder.